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Abstract
The representation of audio, image and video signals involves a vast amount of data, so signal compression is indispensable. Recently, variable length code (VLC) has been widely used in multimedia and lossless coding compression. This thesis describes an efficient class-based VLC Encoder/Decoder and its VLSI architecture. It takes advantage of logic optimization techniques, and achieves high throughput. Besides, it required smaller memory size and it very suitable for applications on the many international image standard, such as JPEG, H.261 and MPEG.

The computation complexity of the VLC is quite low and its memory requirement is small. Hence, it is easily implemented by VLSI and very suitable for real-time applications. An efficient VLSI architecture for VLC is designed and implemented with FPGA chip. It is synthesized with the standard-cell from TSMC's 0.35um cell library. The chip areas are about 1645.2um *1645.2um and 1646um*1646um for the encoder and the decoder respectively. It can achieve about 50Mega symbols/sec encoding/decoding rate.
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